CERTIFICATE OF TRANSMISSION BY FACSIMILE (37 CFR 1.8) Applicant(s): **Timothy J. Dalton, et al.**			Docket No. **YOR920030336US1 (16898)**
Application No. **10/685,012**	Filing Date **October 14, 2003**	Examiner **Jose R. Diaz**	Group Art Unit **2815**

Invention: **PHOTORESIST ASH PROCESS WITH REDUCED INTER-LEVEL DIELECTRIC (ILD) DAMAGE**

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TRANSMITTAL LETTER (General - Patent Pending)	Docket No. YOR920030336US1 (16898)

In Re Application Of: **Timothy J. Dalton, et al.**

Application No.	Filing Date	Examiner	Customer No.	Group Art Unit	Confirmation No.
10/685,012	October 14, 2003	Jose R. Diaz	23389	2815	4288

Title: **PHOTORESIST ASH PROCESS WITH REDUCED INTER-LEVEL DIELECTRIC (ILD) DAMAGE**

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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant(s): Timothy J. Dalton

Examiner: Jose R. Diaz

Serial No: 10/685,012

Art Unit: 2815

Filed: October 14, 2003

Docket: YOR920030336US1 (16898)

For: PHOTORESIST ASH PROCESS WITH REDUCED INTER-LEVEL DIELECTRIC (ILD) DAMAGE

Dated: January 3, 2006

Confirmation No: 4288

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P.O. Box 1450
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DECLARATION PURSUANT TO 37 C.F.R. §1.131

Sir:

We, Timothy J. Dalton, Nicholas C.M. Fuller, and Kaushik A. Kumar, hereby declare that:

1. We are co-inventors of the subject matter described and claimed in the above-identified patent application.

2. Prior to October 10, 2003, which is the effective date of U.S. Patent Application Publication No. 2005/0077597 A1 to Toma, et al. (hereinafter "Toma"), we have conceived and reduced to practice an interconnect structure that comprises a semiconductor substrate comprising one or more device regions and one or more interconnect levels located atop the semiconductor substrate, wherein the one or more interconnect levels comprises a

patterned organosilicate dielectric having sidewalls that comprise CH_x species with x = 1-3, as recited by Claim 1 of the present application.

3. As evidence of the conception and reduction to practice of the claimed interconnect structure referred to in paragraph 2 prior to the effective date of the Toma reference, annexed hereto are Exhibits A and B. Exhibit A is a true photocopy of a write-up for IBM Invention Disclosure YOR8-2003-0269 (hereinafter "Disclosure"), which was created prior to October 10, 2003. Exhibit A describes in general the fabrication of an interconnect structure by using an *in situ* Ar/H_2 plasma ash process (see Exhibit A, page 1, lines 8-12, and page 3, lines 2-4). Specifically, Exhibit A describes that the interconnect structure comprises patterned organosilicate (OSG) dielectric layer with via and/or trench structures therein (see Exhibit A, page 2, lines 10-18), and that the hydrogen atoms provided during the *in situ* Ar/H_2 plasma ash process interacts with the OSG sidewall with a reduced chemical reactivity and forms less volatile CH_x (x = 1-3) species (see Exhibit A, page 3, lines 10-20). Therefore, Exhibit A establishes clear evidence of actual reduction to practice of the claimed interconnect structure as recited by Claim 1 of the present application. Exhibit B is a true photocopy of an email from Nicholas C.M. Fuller attaching an electronic copy of the Disclosure. The email was sent prior to October 10, 2003, thereby evidencing the actual reduction to practice of the claimed interconnect structure prior to the effective date of the Toma reference. All dates on Exhibits A and B have been blacked out in preparation of this Declaration, but which dates are prior to the October 10, 2003 effective date of the Toma reference.

4. We do hereby declare that all statements made herein of our own knowledge are true, and that all statements made on information and belief are believed to be true; and

further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under 18 U.S.C. § 1001, and that such willful false statements may jeopardize the validity or enforceability of the patent.

Dated	Timothy J. Dalton
01/04/06 Dated	Nicholas C.M. Fuller
Dated	Kaushik A. Kumar

further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under 18 U.S.C. § 1001, and that such willful false statements may jeopardize the validity or enforceability of the patent.

29 Dec 2005
Dated

Timothy J. Dalton

Dated

Nicolas C.M. Fuller

Dated

Kaushik A. Kumar

further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under 18 U.S.C. § 1001, and that such willful false statements may jeopardize the validity or enforceability of the patent.

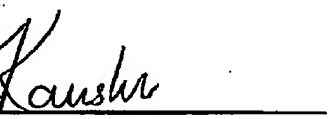
Dated	Timothy J. Dalton
Dated	Nicolas C.M. Fuller
Jan 04, 2006 Dated	 Kaushik A. Kumar

EXHIBIT A

YOR8-2003-0269

PHOTORESIST ASH PROCESS WITH REDUCED INTER-LEVEL DIELECTRIC (ILD) DAMAGE

BACKGROUND

1. Technical Field

The present invention generally relates to integrated circuits (ICs), and more particularly to interconnect structures, including multilevel interconnect structures, in which the original physical and chemical integrity of the dielectric is significantly retained by employing an ash process for photoresist removal post single and dual damascene processing that induces minimal ILD sidewall physical and chemical modification. The present invention is also significant for wafer de-fluorination post barrier (cap) removal during dual damascene processing.

2 Description of Related Art

Generally, semiconductor devices include a plurality of circuits which form an integrated circuit including chips (e.g., chip back end of line, or "BEOL"), thin film packages and printed circuit boards. Integrated circuits can be useful for computers and electronic equipment and can contain millions of transistors and other circuit elements that are fabricated on a single silicon crystal substrate. For the device to be functional, a complex network of signal paths will normally be routed to connect the circuit elements distributed on the surface of the device. Efficient routing of these signals across the device can become more difficult as the complexity and number of the integrated circuits are increased. Thus, the formation of multi-level or multi-layered interconnection schemes such as, for example, dual damascene wiring structures, have become more desirable due

to their efficacy in providing high speed signal routing patterns between large numbers of transistors on a complex semiconductor chip. Within the interconnection structure, metal vias run perpendicular to the silicon substrate and metal lines run parallel to the silicon substrate.

Presently, interconnect structures formed on an integrated circuit chip consists of at least about 2 to 8 wiring levels fabricated at a minimum lithographic feature size designated about 1x (referred to as "thinwires") and above these levels are about 2 to 4 wiring levels fabricated at a width equal to about 2x and/or about 4x the minimum width of the thinwires (referred to as "fatwires"). In one class of structures, the thinwires are formed in a low dielectric constant (k) organosilicate (OSG) dielectric layer, and the fatwires are made in a silicon dioxide dielectric layer having a dielectric constant of about 4.

However, unlike silicon dioxide ILD structures, there are issues associated with retaining the original chemical and physical integrity of OSG materials as the "thinwire" structures are formed during single and dual damascene processing. Specifically, once the "thinwire" structure is formed, in typical "via-first" integration strategies, it is necessary to subsequently remove on the order of 100 to 300nm of photoresist or organic material. Since the via and/or trench structure is present, the resist ash chemistry employed can potentially interact with the exposed OGS sidewall and modify the material properties (which can also occur in some "trench-first" integration strategies where the OSG dielectric is also exposed to the ash chemistry employed). This modified layer can typically be removed leading to increased line-to-line capacitance and via resistance adversely affecting device performance and functionality. If this modified layer is not removed, there may be potential device reliability issues associated with these

structures. It is, thus, necessary to utilize a resist ash process that induces minimal chemical and physical modification of the OSG sidewall. For this purpose we propose the use of an *in situ* Ar/H_2 plasma on the identical commercial etch platform used for via and trench formation during damascene processing. The Ar/H_2 ash process is typically composed of ~90% H_2 and ~10% Ar. Other typical operating conditions on one specific commercial etch platform are: 1 Torr chamber pressure, 500 sccm H_2 and 50 sccm Ar flow, 600 W 27MHz ("Source") Power and <50W 2MHz ("Bias") Power. The process can yield sufficiently quick strip rates (> 120 nm/min) by operating at elevated pressures (1 Torr) and substrate temperatures with only marginal "bias" (substrate) power applied.

Since the plasma in this ash process is ~ 90% hydrogen, hydrogen atoms are the dominant radicals. Two direct routes of OSG material degradation through chemical reactivity include reactivity of exposed Si bonds created during ion impact to the surface and carbon removal from the OSG film. In terms of Si reactivity, the chemisorptive sticking coefficient on Si of hydrogen (<< 0.001) [1] is smaller than that of nitrogen (> 0.05) [2] and oxygen (> 0.1) [2]. As such, a hydrogen-based ash process is likely to have reduced Si chemical reactivity with the OSG sidewall. On the issue of carbon removal, the reaction mechanism for the removal of carbon with oxygen and nitrogen based strip processes is via the formation of CO and CN species respectively. Hydrogen based strip process will likely form various CH_x (x=1-3) species which are less likely to be volatised than CO and CN, thus removing less carbon from the film. Further, on commercial BEOL etch platforms, these ash processes run at pressures > 200 mT, implying that the positive ion mean free path < 0.5 cm [3], [4], i.e. less than the spacing between top and bottom electrodes of most BEOL commercial etch platforms. Ion scattering and, thus, ion impact on the OSG sidewall likely causes physical damage to the OSG material. However, the

dominant ion in these Ar/H_2 plasmas, H^+ (1 amu), will probably cause less damage to the ILD sidewall than O^+ (16 amu) or N^+ (14 amu) because of it's much smaller mass.

The aforementioned physical and chemical properties of this *in situ* Ar/H_2 process, thus facilitates minimized dielectric modification during ashing and consequent desirable device characteristics.

[1] P. Bratu, K. L. Kompa, and U. Höfer *"Optical second-harmonic investigations of H_2 and D_2 adsorption on Si(100)2×1:the surface temperature dependence of the sticking coefficient"* Chem. Phys. Lett. **251**, 1-7 (1996)
[2] D. Graves, Dept. of Chemical Engineering, UC Berkeley, private communication.
[3] N. C. M. Fuller, *Phd Dissertation, "Controlling the Relative Rates of Adlayer Formation and Removal during Etching in Inductively-Coupled Plasmas"* Columbia University (2002)
[4] *Principles of Plasma Discharges and Materials Processing*, edited by M. A. Liebermann and A. J. Lichtenberg (Wiley, New York 1994), pg. 47.

SUMMARY

It is therefore an object of the present invention to provide a BEOL interconnect structure of, e.g., the dual damascene type, in which the original physical and chemical properties of the dielectric are un-altered during ashing in both the thinwire and fatwire levels.

It is a further object of the present invention to provide a BEOL interconnect structure in which both dielectric properties and feature profiles are un-altered during post dual damascene wafer de-fluorination in both thinwire and fatwire levels.

Thus, it is a further object of the present invention to provide a BEOL interconnect structure of improved device functionality, performance, and reliability owing to the reduced demand for removing modified dielectric material.

In keeping with these and other objects of the present invention, there is provided an interconnect structure comprising an organosilicate (OSG) low-k dielectric layer having a set of metallic lines formed therein; such that the surface of the low-k dielectric in contact with the metallic lines is of the original physical and chemical integrity of and matches that of the bulk low-k material facilitating improved device characteristics.

BRIEF DESCRIPTION OF THE DRAWINGS

Preferred embodiments of the present disclosure are described below with reference to the drawings, which are described as follows:

FIG. 1 is a cross sectional SEM showing ash-induced modification of JSR 5109 porous OSG dielectric material utilizing a nitrogen-based de-fluorination process.

FIG. 2 is a cross sectional SEM showing no ash-induced modification of JSR 5109 porous OSG dielectric material utilizing the proposed Ar/H_2 de-fluorination process.

DESCRIPTION OF THE PREFERRED EMBODIMENT

The present invention which is directed to an interconnect structure useful for forming a semiconductor device, the interconnect structure having an unaltered dielectric material physical and chemical properties facilitating improved device performance, functionality, and reliability.

The formation of this structure is made feasible by utilizing an *in situ* Ar/H_2 ash process post via and trench processing in dual damascene scheme that induces minimal chemical and physical modification of the OSG sidewall. The Ar/H_2 ash process is typically composed of ~90% H_2 and ~10% Ar. Other typical operating conditions on one typical commercial etch platform are: 1 Torr chamber pressure, 500 sccm H_2 and 50 sccm Ar flow, 600 W 27MHz ("Source") Power and <50W 2MHz ("Bias") Power. The process yields sufficiently quick strip rates (> 120 nm/min) by operating at elevated pressures (1 Torr) and substrate temperatures with only marginal "bias" (substrate) power applied.

This Ar/H_2 ash process minimizes chemical and physical reactivity with OSG materials owing to its inherent chemical make up: H-radicals are unable to achieve as efficient chemical reactivity with the Si and Carbon within the dielectric film compared with other conventional ash chemistries and the minute ionic mass of H^+ ions ensures minimal physical damage during ion scattering occurring in the ash process.

As a consequence of such a chemically and physically "friendly" ash process, the original chemical and physical integrity of the OSG material is maintained, eliminating the need for removing a modified OSG layer and, further, facilitating improved device performance, functionality and reliability. Further, the characteristics of this process enables its use for post dual damascene wafer de-flourination (DF).

Figure 1
N_2/H_2 DF

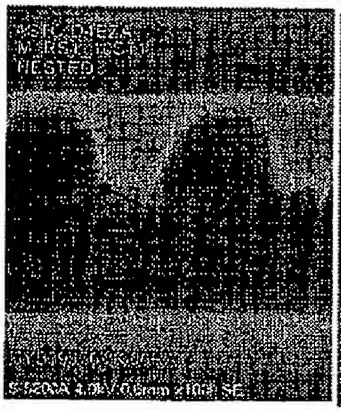
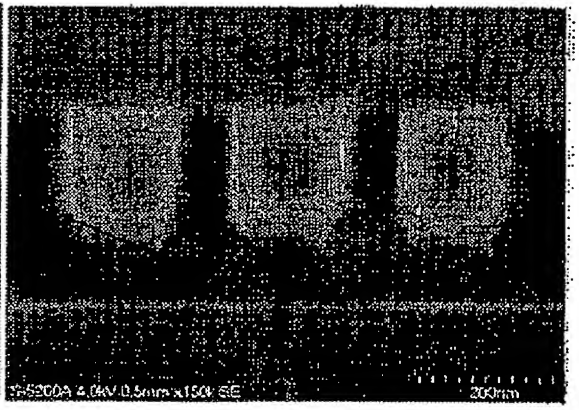


Figure 2
Ar/H_2 DF



ABSTRACT

Novel interconnect structures possessing an organosilicate dielectric material with unaltered physical and chemical material properties post exposure to a specific resist ash chemistry for use in semiconductor devices are provided herein. The novel interconnect structure is capable of delivering improved device performance, functionality and reliability owing to the use of a chemically and physically "friendly" resist ash process. The proposed *in situ* Ar/H_2 process achieves minimal chemical and physical reactivity with the OSG sidewall during ashing owing to its inherent make up; H radicals in the ash chemistry have mild chemical reactivity with the elements in the OSG film and the minute ionic mass of H^+ ions implies minimal physical bombardment of the OSG film during ashing. The proposed chemistry is also particularly useful for post dual damascene wafer de-fluorination for the aforementioned reasons.

EXHIBIT B

Nicholas C Fuller
[redacted]
This document expires on
[redacted]

To: Robert Wisnieff/Watson/IBM@IBMUS, Robert M Trepp/Watson/IBM@IBMUS
cc: Kaushik Kumar/Fishkill/IBM@IBMUS, Timothy Dalton/Fishkill/IBM@IBMUS
From: Nicholas C Fuller/Watson/IBM@ibmus
Subject: Disclosure YOR8-2003-0269

This document contains a file attachment whose file size is: 2.9 MB. Click here to delete all attachments.

Gentlemen

As per our last mtg. to dicuss the above disclosure, the patent has ben written and is attached, please let me know if you have any questions.

Thanks

Photoresist_Ash_Process.doc

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